Abstracts

A Refractory Self-Aligned Gate Process for Monolithically Combined Microwave and Digital GaAs ICs

A. Geissberger, R. Sadler, E. Griffin, I. Bahl, H. Singh and M. Drinkwine. "A Refractory Self-Aligned Gate Process for Monolithically Combined Microwave and Digital GaAs ICs." 1987 MTT-S International Microwave Symposium Digest 87.2 (1987 Vol. II [MWSYM]): 665-668.

We present a process for monolithically fabricating microwave and DCFL digital GaAs circuits. The process employs refractory metal SAG FETs with techniques to provide low gate resistance and high output resistance and break-down voltage. Using a 1.0 µm gate length, 1.5 dB noise figure with 10.2 dB associated gain at 10 GHz analog performance and 65 ps typical propagation delay at 0.5 mW/gate (fan-in/fan-out = 2/2) DCFL digital performance have been obtained.

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